## AMENDMENTS TO THE CLAIMS

Please accept amended Claims 27, and 32-33 as follows:

1-2. (Cancelled)

3. (Previously Presented) A computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising:

a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array;

the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and

wherein the pointer array includes at least one word which is updated based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one word of the pointer array, wherein the entries of the at least one word are updated as part of a same logical operation.

4. (Cancelled)

5. (Previously Presented) A computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising

a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array;

the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and

wherein the pointer array includes at least one word which is updated based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one word of the pointer array, wherein the increment operation includes at least one of a modulo operation and a stride operation.

6. (Original) The system as recited in claim 5, wherein the pointer array includes at least two entries which are updated as part of a same logical operation.

7. (Previously Presented) The system as recited in claim 3, wherein the increment operation includes at least one of a modulo operation and a stride operation.

8. (Previously Presented) The system as recited in claim 3, wherein each entry of the pointer array includes a starting address of at least one storage element in the vector data file.

9. (Previously Presented) A computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising

a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array;

the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and

wherein the storage elements of the vector data file are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array includes an address representing the row and column of at least one element in the vector data file.

10. (Previously Presented) A computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising

a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array;

the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and

wherein the storage elements of the vector file data are logically organized in a matrix of rows and columns, and wherein each array of the pointer array includes an address representing the row and column of a single element in the vector data file.

11. (Previously Presented) A computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising

a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array;

the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and

wherein, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array.

12-13. (Cancelled)

14. (Previously Presented) A computer-implemented method for processing operations that use data vectors each comprising a plurality of data elements, the method comprising the steps of:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, and

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors

stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array; and

updating at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer array, wherein the entries of the of the at least one word are updated as part of a same logical operation.

15. (Cancelled)

16. (Previously Presented) The computer-implemented method as recited in claim 14, wherein the increment operation further includes at least one of a modulo operation and a stride operation on data read from at least one entry of the pointer array.

17. (Previously Presented) The computer-implemented method as recited in claim 16, wherein at least two entries of the pointer array are updated as part of a same logical operation.

18. (Previously Presented) The computer-implemented method as recited in claim 14, wherein the increment operation further includes at least one of a modulo operation and a stride operation on data read from at least one entry of the pointer array.

19. (Previously Presented) The computer-implemented method as recited in claim 14, wherein each entry of the pointer array stores a starting address of at least one storage element in the vector data file.

20. (Previously Presented) The computer-implemented method as recited in claim 14, wherein the storage elements of the vector data file are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array stores an address representing the row and column of at least one element in the vector data file.

21. (Previously Presented) The computer-implemented method as recited in claim 14, wherein the storage elements of the vector file data are logically organized in a matrix of rows and columns, and wherein each array of the pointer array stores an address representing the row and column of a single element in the vector data file.

22. (Previously Presented) The computer-implemented method as recited in claim 14, wherein, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array.

23-24. (Cancelled).

25. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, and

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file; and

updating at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer array, wherein the entries of the of the at least one word are updated as part of a same logical operation.

26. (Cancelled)

27. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, and

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data

vectors, wherein for ~~at least one particular~~ each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data ~~vectors~~ vector stored in the vector data file; and

updating at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer array, wherein the increment operation further includes at least one of a modulo operation and a stride operation on data read from at least one entry of the pointer array.

28. (Original) The program storage device as recited in claim 27, wherein at least two entries of the pointer array are updated as part of a same logical operation.

29. (Previously Presented) The program storage device as recited in claim 25, wherein the increment operation further includes at least one of a modulo operation and a stride operation on data read from at least one entry of the pointer array.

30. (Previously Presented) The program storage device as recited in claim 25, wherein each entry of the pointer array stores a starting address of at least one storage element in the vector data file.

31. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors;

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file,

wherein the storage elements of the vector data file are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array stores an address representing the row and column of at least one storage element of a data vector in the vector data file; and

accessing the vector data file for the data vector, wherein the data vector is addressed according to a word address of the pointer array.

32. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors,

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries having arbitrary starting addresses are grouped into addressable words corresponding to individual data vectors stored in the vector data file; and

wherein the storage elements of the vector file data are logically organized in a matrix of rows and columns, and wherein each ~~array~~ entry of the pointer array stores an address representing the row and column of a single storage element in the vector data file; and

accessing the vector data file for the single storage element to execute an instruction of the program of instructions, wherein the single storage element is addressed according to the address of the pointer array.

33. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising:

providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors,

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data

vectors, wherein for ~~at least one particular~~ each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data ~~vectors~~ vector stored in the vector data file; ~~and~~

wherein, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array; and

performing a read or a write operation that addresses a vector in the vector data file via an index into the pointer array specifying an entry having a plurality of addresses corresponding to different elements of a vector in the vector data file, wherein the read or write operation accesses the vector to execute an instruction of the program of instructions.

34-60. (Cancelled)